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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/567,510	02/07/2006	Hideo Nagai	92478-9800	8521

52044 7590 06/12/2008

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EXAMINER	
HO, HOANG QUAN TRAN	
ART UNIT	PAPER NUMBER
2818	
MAIL DATE	DELIVERY MODE
06/12/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/567,510	NAGAI, HIDEO	
	Examiner	Art Unit	
	Hoang-Quan Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *35-37,40,41 and 46-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *35-37,40,41 and 46-51* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 3, 2008 has been entered.

Response to Amendment

Applicant's amendment to the claims, filed on March 3, 2008, is acknowledged. Entry of amendment is accepted and made of record. Currently, claims 35 – 37, 40 – 41 and 46 – 51 are pending in light of the amendment, in which: claims 35 and 40 – 41 were amended; claims 1 – 34, 38 – 39 and 42 – 45 were cancelled; no claim was withdrawn; and claims 46 – 51 were added.

Response to Arguments/Remarks

Applicant's response filed on March 3, 2008 is acknowledged and is answered as follows.

Applicant's arguments with respect to the rejection of claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 41, 47 and 50 – 51 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 41 recites the limitation "a single-crystal crystal substrate". There is sufficient antecedent basis for this limitation in claim 40.

Claim 47 recites first and second electrodes as n and p type semiconductor materials. Claims 50 – 51 recites the p-electrode, which lack antecedent basis. Furthermore, claim 51 explicitly recites that the second electrode (p-electrode) is formed of Ni/Au and ITO materials. One of ordinary skill in the art would recognize that these materials would not have been proper to be called semiconductor materials, but rather conductive materials. Therefore, the Examiner reasonably takes the position that the first and second electrodes are conductive materials, rather than semiconductor materials.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 35 – 36, 40 – 41, 46 – 48, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durocher et al. (U.S. Pat. No. 6,614,103 B1), hereinafter as Durocher, and further in view of Okazaki et al. (U.S. Pat. App. Pub. No. 2003/0062530 A1), hereinafter as Okazaki.

Regarding claim 35, figs. 12 – 13 of Durocher teaches a semiconductor light emitting device comprising:

a base substrate (ref. no. 41);

a first power supply terminal and a second power supply terminal (one of each ref. 47; col. 9, lines 29 – 31) that are formed on a main surface of the base substrate which faces away from the multilayer epitaxial structure (ref. no. 59; col. 7, lines 30 – 40; see teaching of Okazaki below for multilayer epitaxial structure);

a first conductive member (one of ref. no. 49) including a first through hole (one of ref. no. 37) that is provided in the base substrate (as seen in figs. 12 – 13), and

electrically connecting the first electrode and the first power supply terminal (col. 9, lines 29 – 31; as seen in figs. 12 – 13);

a second conductive member (one of ref. no. 49) including a second through hole (one of ref. no. 37) that is provided in the base substrate (as seen in figs. 12 – 13), and electrically connecting the second electrode and the second power supply terminal (col. 9, lines 29 – 31; as seen in figs. 12 – 13); and

a phosphor film (ref. no. 65) having an even thickness that covers a main surface of the multilayer epitaxial structure which faces away from the base substrate (as seen in figs. 12 – 13, the phosphor film covers the LED chips, ref. no. 59, evenly; see teaching of Okazaki below for multilayer epitaxial structure), and every side surface of the multilayer epitaxial structure from a layer including the main surface to include at least the light emitting layer (as seen in figs. 12 – 13; see teaching of Okazaki below for multilayer epitaxial structure).

Durocher may not explicitly teach the following limitations whereas figs. 1 and 3D of Okazaki teaches it is known in the art to provide:

a multilayer epitaxial structure (¶0049) includes a first conductive layer (ref. no. 2), a second conductive layer (ref. no. 4) and a light emitting layer (ref. no. 3) that is formed between the first conductive layer and the second conductive layer (as seen in fig. 1),

the multilayer epitaxial structure being formed on the base substrate in such a manner that the first conductive layer is positioned closer to the base substrate than the

second conductive layer is (as combined with the teaching of figs. 12 – 13 of Durocher and fig. 3A of Okazaki);

a first electrode (ref. no. 5) that is formed on the first conductive layer (as seen in fig. 1);

a second electrode (ref. no. 13) that is formed on the second conductive layer (as seen in fig. 1);

an insulating film (ref. no. 7) that covers side surfaces of the multilayer epitaxial structure and separates the first electrode and the second electrode (as seen in fig. 3D).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the invention of Durocher with the light emitting device of Okazaki, in order to provide improved external quantum efficiency light emitting devices (¶0040). It is proper to combine Durocher and Okazaki because they both teach analogous art relating to light emitting devices.

Regarding claim 36, Durocher and Okazaki teaches the semiconductor light emitting device of Claim 35, Durocher teaches wherein the multilayer epitaxial structure is formed on the base substrate leaving a space along each edge of a main surface of the base substrate which faces the multilayer epitaxial structure (as seen in fig. 12, next to each LED, ref. no. 59, are spaces); and

the first through hole and the second through hole are provided in a peripheral portion of the base substrate, the peripheral portion corresponding to the space (as seen in fig. 12, at the left and the right peripheral sides of the LEDs).

Regarding claim 40, Durocher and Okazaki teaches the semiconductor light emitting device of Claim 35, Durocher and Okazaki teaches wherein the multilayer epitaxial structure having a structural characteristic of epitaxial growth (¶0049 of Okazaki) on a single-crystal substrate (ref. no. 1 and ¶0039 of Okazaki) different from the base substrate (col. 5, lines 17 – 31 of Durocher), and is mounted on the base substrate (as combined and would have been seen just as figs. 12 – 13 of Durocher with fig. 1 of Okazaki).

Regarding claim 41, Durocher and Okazaki teaches the semiconductor light emitting device of Claim 40, Durocher and Okazaki teaches wherein the multilayer epitaxial structure is mounted to the base substrate in such a manner that a last epitaxially-grown layer (ref. no. 2 of Okazaki; see note 1 below) having grown on a single-crystal substrate (ref. no. 1 and ¶0039 of Okazaki) different from the base substrate is positioned closer to the base substrate than a first epitaxially-grown layer (ref. no. 4 of Okazaki; see note 1 below) is.

Note 1: The recited limitation is drawn to a process by which the product is made. Even though product by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product by process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. Because

the product by process does not change the end product, Applicant's claimed invention does not distinguish over prior art. See MPEP § 2113.

In the instant case, the first and last epitaxially-grown layers as recited are oppositely grown by what is taught by ¶0049 of Okazaki. Okazaki teaches that ref. no. 2 layer was one of the first to grow and ref. no. 4 is grown thereafter. However, chronological ordering of when the layers are epitaxially-grown would not have changed the end result of the product, as Okazaki's end product rendered the claimed invention obvious.

Regarding claim 46, Durocher and Okazaki teaches the semiconductor light emitting device of Claim 35, Durocher teaches wherein the first and the second through holes are positioned in a periphery of the base substrate (as seen in fig. 12, next to each LED, ref. no. 59, are spaces at the left and the right peripheral sides of the LEDs), and the multilayer epitaxial structure is not positioned on or over the first and second through holes (as seen in fig. 12).

Regarding claim 47, figs. 12 – 13 of Durocher teaches a semiconductor light emitting device comprising:

a base substrate (ref. no. 41);

a first power supply terminal and a second power supply terminal (one of each ref. 47; col. 9, lines 29 – 31) that are formed on a main surface of the base substrate

which faces away from the multilayer epitaxial structure (ref. no. 59; col. 7, lines 30 – 40; see teaching of Okazaki below for multilayer epitaxial structure);

a first conductive member (one of ref. no. 49) including a first through hole (one of ref. no. 37) that is provided in the base substrate (as seen in figs. 12 – 13), and electrically connecting the first electrode and the first power supply terminal (col. 9, lines 29 – 31; as seen in figs. 12 – 13);

a second conductive member (one of ref. no. 49) including a second through hole (one of ref. no. 37) that is provided in the base substrate (as seen in figs. 12 – 13), and electrically connecting the second electrode and the second power supply terminal (col. 9, lines 29 – 31; as seen in figs. 12 – 13); and

a phosphor film (ref. no. 65) that covers a main surface of the multilayer epitaxial structure which faces away from the base substrate (as seen in figs. 12 – 13, the phosphor film covers the LED chips, ref. no. 59, evenly; see teaching of Okazaki below for multilayer epitaxial structure), and every side surface of the multilayer epitaxial structure from a layer including the main surface to include at least the light emitting layer (as seen in figs. 12 – 13; see teaching of Okazaki below for multilayer epitaxial structure).

Durocher may not explicitly teach the following limitations whereas figs. 1 and 3D of Okazaki teaches it is known in the art to provide:

a multilayer epitaxial structure (¶0049) includes a first conductive layer (ref. no. 2), a second conductive layer (ref. no. 4) and a light emitting layer (ref. no. 3) that is

formed between the first conductive layer and the second conductive layer (as seen in fig. 1),

the multilayer epitaxial structure being formed on the base substrate in such a manner that the first conductive layer is positioned closer to the base substrate than the second conductive layer is (as combined with the teaching of figs. 12 – 13 of Durocher and fig. 3A of Okazaki);

a first electrode (ref. no. 5) that is formed on the first conductive layer (as seen in fig. 1) as an n-type semiconductor layer (¶0039);

means for improving the light extraction efficiency (¶0040) including a second electrode (ref. no. 13) that is formed on the second conductive layer as a p-type semiconductor layer (¶0039) with an uneven surface (as seen in fig. 1).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the invention of Durocher with the light emitting device of Okazaki, in order to provide improved external quantum efficiency light emitting devices (¶0040). It is proper to combine Durocher and Okazaki because they both teach analogous art relating to light emitting devices.

Regarding claim 48, Durocher and Okazaki teaches the semiconductor light emitting device of Claim 47, Durocher and Okazaki teaches wherein the multilayer epitaxial structure is mounted on the base substrate in such a manner that a last epitaxially-grown layer (ref. no. 2 of Okazaki; see note 1 below) having a structure characteristic (¶0049 of Okazaki) of being grown on a single-crystal substrate (ref. no. 1

and ¶0039 of Okazaki) different from the base substrate (col. 5, lines 17 – 31 of Durocher) is positioned closer to the base substrate (as combined and would have been seen just as figs. 12 – 13 of Durocher with fig. 1 of Okazaki) than a portion of a first epitaxially-grown layer (ref. no. 4 of Okazaki; see note 1 below).

Note 1: The recited limitation is drawn to a process by which the product is made. Even though product by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product by process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process. Because the product by process does not change the end product, Applicant's claimed invention does not distinguish over prior art. See MPEP § 2113.

In the instant case, the first and last epitaxially-grown layers as recited are oppositely grown by what is taught by ¶0049 of Okazaki. Okazaki teaches that ref. no. 2 layer was one of the first to grow and ref. no. 4 is grown thereafter. However, chronological ordering of when the layers are epitaxially-grown would not have changed the end result of the product, as Okazaki's end product rendered the claimed invention obvious.

Regarding claim 50, Durocher and Okazaki teaches the semiconductor light emitting device of Claim 47, Okazaki teaches wherein a plurality of depressions is

formed on a surface of the p-electrode surface to improve light extraction efficiency (¶0040; as seen in figs. 1 and 3D).

Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Durocher and Okazaki as applied to claim 35 above, and further in view of Baik et al. (U.S. Pat. App. Pub. No. 2004/0108511 A1), hereinafter as Baik.

Regarding claim 37, Durocher and Okazaki teaches the semiconductor light emitting device of Claim 35, but Durocher and Okazaki may not explicitly teach the following limitations whereas Baik teaches that it is known in the art to provide further comprising:

a metal reflective film (ref. nos. 35, 37 and/or 39) that is sandwiched between the multilayer epitaxial structure (ref. nos. 24, 26 and 28) and the base substrate (Durocher's ref. no. 41 as seen in figs. 12 – 13).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the invention of Durocher and Okazaki with the reflective film of Baik, in order to provide excellent reflective characteristics (¶0018). It is proper to combine Durocher, Okazaki and Baik because they both teach analogous art relating to light emitting devices.

Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Durocher and Okazaki as applied to claim 47 above, and further in view of Baik et al. (U.S. Pat. App. Pub. No. 2004/0108511 A1), hereinafter as Baik.

Regarding claim 49, Durocher and Okazaki teaches the semiconductor light emitting device of Claim 47, but Durocher and Okazaki may not explicitly teach wherein the base substrate is a SiC substrate. However, Durocher teaches that the base substrate (ref. no. 41) could be made from a flexible carrier, glass circuit board or the like (col. 5, lines 17 – 31 of Durocher). Furukawa teaches that it is known in the art to provide wherein the base substrate is a SiC substrate (¶0773). It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the invention of Durocher with the substrate material of Furukawa, in order to provide an alternative substrate material. It is proper to combine Durocher and Furukawa because they both teach analogous art relating to LED structure and the substrate materials.

Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Durocher and Okazaki as applied to claim 50 above, and further in view of Lee et al. (U.S. Pat. App. Pub. No. 2003/0190764 A1), hereinafter as Lee.

Regarding claim 51, Durocher and Okazaki teaches the semiconductor light emitting device of Claim 50, Okazaki teaches wherein a Ni thin film and an ITO

transparent electrode form the p-electrode (¶0059). But Okazaki may not explicitly teach a Ni/Au thin film. ¶0014 of Lee teaches that it is known in the art to provide a Ni/Au/ITO as a p-type ohmic electrode in a GaN based device. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the invention of Okazaki with the Ni/Au thin film of Lee, in order to decrease contact resistance (¶0014). It is proper to combine Okazaki and Lee because they both teach analogous art relating to light emitting device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoang-Quan Ho whose telephone number is 571-272-8711. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Loke can be reached on 571-272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HQH/
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June 9, 2008

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